IN THE SPECIFICATION

Amend the specification as follows.

At page 4, lines 11-21, replace the third paragraph with the following.

B1

—The input and output mode set circuit comprises a mode register set circuit and is adapted to receive a group of the plurality of mode register address signals and first and second internal signals and adapted to generate first and second mode register signals responsive to the group of mode register address signals and the first and second internal signals. A control signal generating circuit is adapted to generate a plurality of control signals responsive to the first and second mode register signals, a remaining group of the plurality of mode register address signals, the first internal signal, and a third internal signal. An input and output mode signal generator is adapted to receive the plurality of control signals, cut off signals the plurality of external control signals responsive to at least one of the plurality of control signals, and generate the plurality of input and output mode signals responsive to the remaining control signals.—

At page 7, lines 12-19, replace the third paragraph with the following.

B2

—When a high voltage, for example, 8 volts is applied to the pad 251, since the PMOS transistors 311 through 314 are turned on, the voltage level of node N3 is increased to 5.2 volts. The threshold voltage of the PMOS transistors 311 through 314 is 0.7 volts. The PMOS transistors 311 through 314 are much smaller than the NMOS transistor 341. Therefore, the first signal SV4 is activated to a logic high level. ~~The~~ When the high voltage is applied to the pad 252 by the same principle, the second signal SV8 is activated to the logic high level. When the high voltage is applied to the pad 253, the third signal SV16 is activated to the logic high level.—

At page 9, lines 10-19, replace the second paragraph with the following.

B3

—Referring to FIGS. 3 and 4, when the supply voltage Vcc is applied to the semiconductor memory device 201 and the high voltage is applied to the pad 251, the signals ORGS1 and MFE are at the logic high level. The signals ORGS1 and MFE are maintained at the logic high level although the high voltage is not applied to the pad 251. Namely, the signals ORGS1 and MFE may be continuously generated at the logic high level although the high voltage is applied to the pad 251 only for a short period of time. ~~The~~ Likewise, the signals ORGS2 and ORGSM are continuously ~~hold~~ held at the logic high level although the high voltage is applied to the pad 252 for a short period of time. The signals ORGS3, MHE, and ORGSM are continuously ~~hold~~ held at the logic high level although the high voltage is applied to the pad 253 for a short period of time.—

At page 10, lines 23-28, replace the second paragraph with the following.

B4

—When the second and third control signals MFE and MHE are deactivated to the logic low level in a state where the first control signal ORGSM is at the logic high level, the input and output mode signals P4 and P16 remain at the logic low level. Therefore, the input and output mode of the semiconductor memory device 201 is set to ×8. The second and third

B4

control signals MFE and MHE are never both at the logic high level when the first control signal ORGSM is at the logic high level.—

At page 11, line 30 to page 12 line 13, replace the last paragraph with the following.

B5

—The mode register set circuit 621 is shown in detail in FIG. 7. Referring to FIG. 7, the mode register set circuit 621 includes NOR gates 711 and 712, NAND gates 731 through 734, and inverters 721 through 724. The mode register set circuit 621 receives mode register address signals MRA4B through MRA8B, the power supply sense signal PVCCH, and the second internal signal PWCBR and generates first and second mode register signals ORGSET and MRSET, respectively. In order to activate the first mode register signal ORGSET to the logic high level, the mode register address signals MRA4B through MRA7B and the second internal signal PWCBR must be activated to the logic high level and the mode register address signal MRA8B must transition to the logic low level. When the mode register address signal MRA7B is at the logic high level and the mode register address signal MRA8B is at the logic low level, the output of the NOR gate 711 is at the logic high level. Also, when the mode register address signals MRA4B through MRA6B are at the logic high level, the output of the inverter 723 transitions to the logic high level. In this state, when the second internal signal PWCBR is activated to the logic high level, since signals input to the NAND gate 732 are at the logic high level, the first mode register signal ORGSET is activated to the logic high level. Here, the NAND gate 732 and the inverter 724 operate as an AND circuit.—

At page 12, lines 26-33, replace the second paragraph with the following.

B6

—The control signal generating circuit 631 is shown in detail in FIG. 8. Referring to FIG. 8, the control signal generating circuit 631 includes PMOS transistors 811 and 814 through 815, ~~an~~ NMOS transistors 811 through 813 and 851, transmission gates 821 through 825, inverters 831 through 836, latch circuits 841 through 845, a NAND gate 861, and buffers 871-872. The control signal generating circuit 631 receives the power supply sense signal PVCCH, the first and second mode register signals ORGSET and MRSET, a third internal signal PMRSPD, and mode register address signals MRA9B and MRA10B and generates the first through third control signals ORGSM, MHE, and MFE.—

At page 13, lines 23-31, replace the second paragraph with the following.

B7

—As shown in FIG. 10, the third internal signal ~~PMRSPD~~ PMRSP is activated to the logic high level when the clock signal CLK transitions from the logic low level to the logic high level in a state where the write enable signal WEB, the row address strobe signal RASB, and the column address strobe signal CASB are at the logic low level. Also, the third internal signal ~~PMRSPD~~ PMRSP is deactivated to the logic low level when the clock signal CLK transitions from the logic low level to the logic high level in a state where one of the write enable signal WEB, the row address strobe signal RASB, and the column address strobe signal CASB is at the logic high level. The third internal signal ~~PMRSPD~~ PMRSP can be replaced by the second internal signal PWCBR.—

At page 15, lines 13-25, replace the second paragraph with the following.

—When the third control signal MHE is at the logic ~~low~~ high level in a state where the first control signal ORGSM is at the logic high level, the transmission gate 916 is turned off and the transmission gate 918 is turned on since the output of the inverter 925 is at the logic low level. Therefore, since a node N8 is at the ground voltage GND level, which is inverted by the inverters 926 through 928, the input and output mode signal P16 is at the logic high level. When the third control signal MHE is at the logic ~~low~~ high level, the transmission gate 918 is turned on and the transmission gate 916 is turned ~~on~~ off. Therefore, since a node N8 is at the ground voltage GND level, which is inverted by the inverters 926 through 928, the input and output mode signal P16 is enabled to the logic high level. When the third control signal MHE is at the logic low level, the transmission gate 918 is turned off and the transmission gate 916 is turned on. Therefore, since the node N8 is at the supply voltage Vcc level, which is inverted by the inverters 926 through 928, the input and output mode signal P16 is disabled to the logic low level.—

P58